LISTING OF THE CLAIMS (16-35)

Claim 16 (previously amended): A method for fabricating a semiconductor device with a trenched gate comprising:

forming an oxide layer on the surface of a semiconductor substrate;

forming a nitride layer on said oxide layer;

etching a trench having substantially upright vertical sidewalls and a bottom surface in said semiconductor substrate;

forming a trench-to-gate insulating layer inside the trench, wherein the trench-to-gate insulating layer comprises a trench gate dielectric spacer formed on the upright vertical sidewalls inside the trench and a trench gate tunneling dielectric formed on the bottom surface inside the trench;

forming a trenched gate electrode on the trench-to-gate insulating layer inside the trench;

forming a source region and a drain region in the semiconductor substrate such that the source and drain regions partially extend laterally underneath the bottom of the trench;

~~forming sidewall dopings on the sidewalls to reduce coupling~~ between the control gate and the source and drain regions;

forming an inter-gate dielectric layer on a top surface of the trenched gate electrode; and

forming a control gate electrode on a top surface of the inter-gate dielectric layer.

Claim 17 (original): The method of Claim 16 wherein the step of forming a trenched gate electrode further comprises the steps of:

depositing a layer of polysilicon on the trench-to-gate insulating layer inside the trench; and

planarizing the layer of polysilicon to substantially planar orientation with a top surface of the semiconductor substrate.

Claim 18 (original): The method of Claim 16 further comprising the step of implanting the semiconductor substrate to form sidewall dopings in the substrate laterally spacing each of the source and drain regions from the trench.

Claim 19 (previously amended): A method for fabricating a semiconductor device with a trenched gate comprising:

etching a trench having substantially upright vertical sidewalls and a bottom surface in a semiconductor substrate;

forming a trench-to-gate insulating layer inside the trench, wherein the trench-to-gate insulating layer comprises a trench gate dielectric spacer formed on the upright vertical sidewalls inside the trench and a trench gate tunneling dielectric formed on the bottom surface inside the trench;

forming a trenched gate electrode on the trench-to-gate insulating layer inside the trench;

forming a source region and a drain region in the semiconductor substrate such that the source and drain regions partially extend laterally underneath the bottom of the trench;

forming an inter-gate dielectric layer on a top surface of the trenched gate electrode;

forming a control gate electrode on a top surface of the inter-gate dielectric layer, and

wherein the step of forming a source region and a drain region comprises corner-limiting diffusion process.

Claim 20 (original): The method of Claim 16 further comprising, after etching the trench in the semiconductor substrate, forming ~~sidewall dopings in the semiconductor substrate~~ by implanting the semiconductor substrate with dopant impurities at an angle which is approximately between 15 and 75 degrees.

Claim 21 (previously presented): The method of Claim 16, wherein said nitride is silicon nitride.

Claim 22 (previously presented): The method of Claim 21, wherein said nitride is approximately 1500 angstroms thick.

Claim 23 (previously presented): The method of Claim 16, wherein said oxide layer is approximately 100 angstroms thick.

Claim 24 (previously presented): The method of Claim 16, further comprising planarizing said trenched gate electrode using said nitride as a stop for the planarization process.

Claim 25 (previously presented): The method of Claim 24, further comprising removing said nitride layer using a plasma etch.

Claim 26 (previously presented): The method of Claim 16, wherein said trench is between approximately 100 angstroms and 5000 angstroms wide.

Claim 27 (previously presented): The method of Claim 16, wherein said trench is between approximately 100 angstroms and 5000 angstroms deep.

Claim 28 (previously presented): The method of Claim 19, further comprising:

forming an oxide layer on the surface of said semiconductor substrate; and

forming a nitride layer on said oxide layer.

Claim 29 (previously presented): The method of Claim 28, wherein said nitride is silicon nitride.

Claim 30 (previously presented): The method of Claim 29, wherein said nitride is approximately 1500 angstroms thick.

Claim 31 (previously presented): The method of Claim 28, wherein said oxide layer is approximately 100 angstroms thick.

Claim 32 (previously presented): The method of Claim 28, further comprising planarizing said trenched gate electrode using said nitride as a stop for the planarization process.

Claim 33 (previously presented): The method of Claim 28, further comprising removing said nitride layer using a plasma etch.

Claim 34 (previously presented): The method of Claim 28, wherein said trench is between approximately 100 angstroms and 5000 angstroms wide.

Claim 35 (previously presented): The method of Claim 28, wherein said trench is between approximately 100 angstroms and 5000 angstroms deep.